INFLUENCE OF PYRAMID SIZE OF CHEMICALLY TEXTURED SILICON WAFERS ON THE CHARACTERISTICS OF INDUSTRIAL SOLAR CELLS

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ABSTRACT: Pyramidal texture on monocrystalline silicon wafers is a very common surface structure of industrial monocrystalline silicon solar cells because of its advantage to reduce light reflection. However, pyramidal texture with big pyramids (15 μ m) or small pyramids (0.3 μ m) produce lower performance of solar cells. By using a wet chemical method we produced a pyramidal texture on (100) p-type Czochralski monocrystalline silicon wafers. We achieved pyramidal texture with pyramid size between 1 μ m and 6 μ m. After that, we processed industrial silicon solar cells by using the screen printing method. Solar cells achieved efficiencies between 16.7 % and 17.7 %. Keywords: Texturisation, silicon, solar cells

1 INTRODUCTION

In the industrial production of monocrystalline silicon (Si) solar cells the texturing of silicon wafers is a very common process. The texturing is usually carried out by a wet chemical method, which uses water, potassium hydroxide (KOH) and isopropyl alcohol (IPA). Due to the anisotropy of this method, small pyramids are formed on the silicon surface (pyramidal texture). Pyramids are constituted by four triangles on the (111) planes and a square base on the (100) plane. This pyramidal texture increases the area of a planar Si wafer 1.7 times, in two dimensions, it can be obtained by calculation of the hypotenuse *h* (enlargement) of the triangle formed by the (100) and (111) planes; $h = 1/cos(\Theta)$, where $\Theta = 54.7^{\circ}$ corresponds to the angle between the planes.

Pyramidal texture on Si wafers reduces total light reflection and therefore an increase on short circuit current of solar cells is generally observed. However, larger or very small pyramids result in lower performance of solar cells. Large pyramids, larger than 15 µm, could lead to their breaking during handling [1]. On the other side, very small pyramids, smaller than 0.3 µm, result in an increase of reflection values because light diffraction becomes apparent in the long wavelength range [2]. Therefore, we are interested to study the influence of pyramidal texture with different pyramid size on the performance of industrial screen printed Si solar cells. In order to obtain a pyramidal texture with pyramid size between 1 µm and 6 µm we varied the etching time of Si wafers. After etching, reflection measurements were carried out and Scanning Electron Microscope (SEM) pictures were taken. Then, textured silicon wafers were processed to solar cells by using the industrial screen printing method.

2 EXPERIMENTAL

We used 12.5x12.5 cm² p-type Czochralski silicon wafers (Cz-Si) with (100) orientation. The resistivity was $1-3 \Omega$ cm. The etching process was carried out in two steps. First, silicon wafers were etched 4 min in a concentrated (22%) sodium hydroxide (NaOH) etching solution at 80 °C. After this etching process 15 µm of silicon (7.5 µm per side) were removed from silicon wafers and a "planar surface" without almost any saw damage was obtained (see figure 2a). Second, the Si wafers were etched in an texturing solution which consists of 6 liters of deionized water, potassium hydroxide (KOH) and a high boiling alcohol (HBA) at 100 °C (KOH-HBA solution). We varied the etching time between 10 and 30 min in order to change the pyramid size. After this etching process $3 - 9 \,\mu$ m of silicon (1.5 – 4.5 μ m per side) were removed from silicon wafers. We used the same KOH-HBA etching solution five times (batch size: 20 wafers) and we dosed only water during the etching process. To characterize the pyramidal texture on Si wafers, reflection measurements were carried out and Scanning Electron Microscope (SEM) pictures were taken. Silicon removal was calculated by weighing silicon wafers before and after etching processes.

After the texturing process, a phosphorous diffusion (POCl₃) process formed an emitter with a sheet resistance of 50 Ω /sq on textured Si wafers. Then, by using the plasma-enhanced chemical vapor deposition (PECVD) method a silicon nitride (SiN_x:H, d = 75 nm, n = 2.0) layer was deposited on the emitter as antireflection coating. After that, silver front and aluminum back contacts were screen printed, and a co-firing step was carried out. Finally, edges of solar cells were isolated by sawing. After production of solar cells, current-voltage measurements under AM 1.5 illumination conditions were carried out.

3 RESULTS

Figure 1 shows SEM pictures of an as-cut silicon wafer. The saw damage on this Si wafer penetrates approximately $10 \,\mu\text{m}$ deep into the wafer, as it can be seen from the left side of figure 1 (cross sectional view of the wafer). Therefore, by an etching process $10 \,\mu\text{m}$ per side of the Si wafer should to be removed. On the right side of figure 1, a SEM picture of the surface of an as-cut Si wafer is shown.

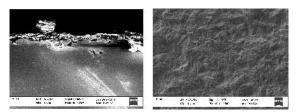


Figure 1: SEM picture of an as-cut silicon wafer (left: cross section, right: plan view). Saw damage penetrates approximately $10 \,\mu$ m deep into the wafer.

Figure 2 shows a SEM picture of etched silicon wafers. Figure 2a) corresponds to an as-cut silicon wafer etched 4 minutes in a high concentrated sodium hydroxide (NaOH) solution. Figures 2 b-f) correspond to silicon wafers which first were etched in the high concentrated NaOH solution and then were etched in a KOH-HBA solution. From figure 2 we observe that pyramid size increases as etching increases from 0 to 15 min. By etching 20 min pyramid size is getting smaller again. However, etching times longer than 20 min decrease and increase pyramid size simultaneously. Small and large pyramids reach sizes below 300 nm and over 4 μ m, respectively, see figure 2 f).

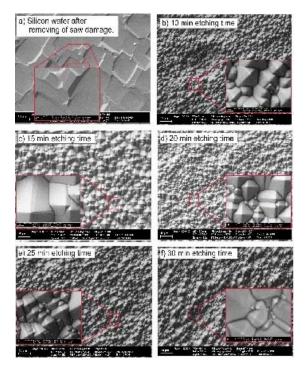


Figure 2: SEM pictures of Si wafers etched in a NaOH (Figure 2 a)) and afterwards in KOH-HBA (Figure 2 b-f)) etching solutions.

Figure 2 a) shows a silicon wafer etched 4 min in a 22 % concentrated sodium hydroxide (NaOH) etching solution at 80 °C. After etching, an almost flat surface ("planar texture") was obtained. Figure 2 b-f) shows the SEM pictures of pyramidal texture obtained after further etching silicon wafers 10, 15, 20, 25, and 30 min in a KOH-HBA texturing solution at 100 °C, respectively. Figure 2 b) shows the surface of a silicon wafer etched 10 min, the pyramidal texture shows small pyramids with rounded corners. The pyramid size varies between 1-4 µm. Such a pyramidal texture considerably decreases light reflection (see figure 3). Figure 2 c) corresponds to a silicon wafer which was etched 15 min. A sufficiently homogeneous texture with big pyramids is observed. Pyramid sizes vary from 3 to 6 µm. From this figure, only few small pyramids can be observed. Figure 2 d) shows the surface of a silicon wafer etched 20 min. A sufficiently homogeneous pyramidal texture with

pyramid size between 1 and 4 μ m is observed. This pyramidal texture produces the lowest total light reflection (see figure 3). Figure 2 e) shows a Si wafer etched 25 min. An inhomogeneous pyramidal texture with a lot of small pyramids (0.2-1 μ m) and only few big pyramids (4 – 5 μ m) is observed. This pyramidal texture slightly increases light reflection with respect to the texture of figure 2 d). Figure 2 f) shows a Si wafer etched for 30 min, an inhomogeneous pyramidal texture with more large pyramids (5-6 μ m) than small pyramids (0.2-1 μ m) is observed. This pyramidal texture again slightly enhances light reflection, but reflection values do not exceed 10 % (at a wavelength of 900 nm).

Figure 3 shows reflection measurements of Si wafers which first were etched 4 min in a high concentrated sodium hydroxide (NaOH) solution at 80 °C and then were etched 10, 15, 20, 25 and 30 min in a texturing solution which consists of water, potassium hydroxide (KOH) and a High Boiling Alcohol (HBA) at 100 °C.

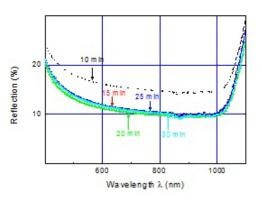


Figure 3: Reflection measurements of silicon wafers which first were etched in a high concentrated NaOH solution and then etched in a KOH-HBA texturing solution. After 15 min of etching time reflection values decrease below 10 % (at 850 nm $< \lambda < 1000$ nm).

From this figure, we observe a decrease of reflection by increased etching times, however, etching times longer than 20 min do not reduce total light reflection of textured Si wafers any more. In contrary, a longer etching time slightly increases light reflection but light reflection values can be kept below 10 % (at 850 nm $< \lambda < 1000$ nm). For Si wafers textured for only 10 min. reflection of around 14 % а (at 850 nm $< \lambda < 1000$ nm) is observed.

From these textured wafers we processed solar cells by using the screen printing method. Figure 4 shows the current-voltage (IV) characteristics of the cells as a function of the etching time of the wafers.

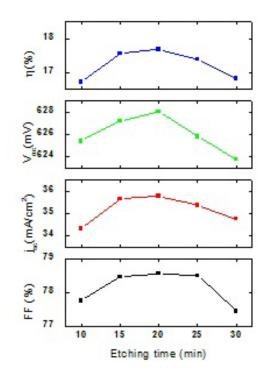


Figure 4: Current-voltage (IV) characteristics of screen printed Cz silicon solar cells $(12.5x12.5 \text{ cm}^2)$ processed from Si wafers with varying texturing time.

From figure 4, we observe that solar cells produced with Si wafers etched for 15, 20, and 25 min achieve solar cell efficiencies higher than 17 %, whereas solar cells processed from Si wafers etched for 10 and 30 min reach cell efficiencies below 17 %. The highest solar cell efficiency of 17.7 %, was obtained from wafers which were etched 20 min, which correspond to homogeneous pyramidal texture with pyramid size of $1-4 \mu m$, respectively. Discussion of the IV characteristics of these solar cells is given below.

4 DISCUSSION

From figure 4 we see that the short circuit current density (j_{sc}) has the lowest value for solar cells produced from Si wafers which were etched only 10 min. This i_{sc} value is in agreement with the high reflection values of the texture. For etching times longer than 10 min an increase in j_{sc} is observed and it reaches a maximum value of $j_{sc} = 35.8 \text{ mA/cm}^2$ for an etching time of 20 min. Such maximum j_{sc} value is in agreement with the lowest reflection values observed for these textured Si wafers (see figure 3). For longer etching times a constant decrease in j_{sc} is observed. In general, the decrease of j_{sc} can be assigned to a slightly increase on reflection values. For an etching time of 30 min a decrease of the long wavelength of the Internal Quantum Efficiency (IQE) was observed (not shown here). This is in agreement with the lower j_{sc} values, but the origin of this behavior is still unclear.

From figure 4, we observe that the fill factor (*FF*) of solar cells increases with increasing etching times and reaches its maximum value FF = 78.6 % for solar cells

produced with Si wafers etched for 20 min. These solar cells have sufficiently homogeneous pyramidal texture with small pyramid size (1-4 μ m). Longer etching time decreases the *FF* of solar cells.

From figure 4, we observe an increase of the open circuit voltage (V_{oc}) between 10 and 20 min of etching time. For an etching of 20 min V_{oc} takes its highest value of $V_{oc} = 628$ mV. An etching time of 20 min produces a sufficiently homogeneous pyramidal texture with small pyramids (1-4 µm) on Si wafers.

Table I shows characteristics of solar cells processed with pyramidal structure with different pyramid size.

Table I: Current-voltage results of screen printed Cz silicon wafers $(125x125 \text{ mm}^2)$ produced from Si wafers etched different times in a KOH-HBA texturing solution (averaged over 20 cells).

Etching	Pyramid	j_{sc}	V_{oc}	FF	η
time	size	(mA/cm^2)	(mV)	(%)	(%)
(min)	(µm)				
10	1-4	34.3	625.4	77.8	16.7
15	3-6	35.6	627.2	78.5	17.6
20	1-4	35.8	628.0	78.6	17.7
25	1-5	35.4	625.8	78.5	17.4
30	1-6	34.8	623.8	77.4	16.8

Thus, we conclude that solar cells produced with: a) sufficiently homogeneous pyramidal texture with pyramid size between 3-6 μ m (15 min), b) sufficiently homogeneous pyramidal texture with pyramid size between 1-4 μ m (20 min) and c) pyramidal texture with a lot of small pyramids (1 μ m) and few large pyramids (5 μ m) (25 min) result in better performance of solar cells. On the other side, solar cells produced with: a) pyramidal texture with "rounded pyramids" with sizes between 1-4 μ m (10 min) and b) inhomogeneous pyramidal texture with a combination of both a few small (1 μ m) and a lot of large pyramids (6 μ m) (30 min) result in lower performance of solar cells.

5 SUMMARY

In order to study the influence of pyramid size of chemically textured Si wafers on the characteristics of industrial solar cells we processed solar cells from silicon wafers with varying texturing time. The texturing process was carried out in two steps. First, Si wafers were etched during 4 min in a high concentrated (22 %) sodium hydroxide (NaOH) solution at 80 °C. Second, the Si wafers were etched in a texturing solution which consists of 6 liters of deionized water, potassium hydroxide (KOH) and a high boiling alcohol (HBA) at 100 °C (KOH-HBA etching solution), in this step, etching time was varied between 10 and 30 min in order to change pyramid size. Textured Si wafers show rounded, homogeneous and inhomogeneous pyramidal texture with pyramid size between 1 and 6 µm. Etching times longer than 15 min decreases reflection values below 10 % at 850 nm $< \lambda < 1000$ nm. The lowest reflection values were obtained from Si wafers etched for 20 min.

After the texturing process of Si wafers, they were processed to solar cells by using the screen printing method. Sufficiently homogeneous pyramidal texture with pyramid size of $3-6\,\mu\text{m}$ (15 min) and $1-4\,\mu\text{m}$ (20 min) allows solar cells to achieve efficiencies of 17.6% and 17.7%, respectively. Whereas rounded pyramidal texture with pyramid size of $1-4\,\mu\text{m}$ (10 min) and inhomogeneous pyramidal texture with pyramid size of $1-6\,\mu\text{m}$ (30 min) achieve efficiencies below 17%.

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7 REFERENCES

- [1] F. Hernando, R. Gutiérrez, G. Bueno, F. Recart, V. Rodríguez, "Humps, a surface damage explanation", Proc. 2nd WC PEC, Vienna, (1998) 1321.
- [2] F. Llopis, I. Tobias, "Influence of texture feature size on the optical performance of silicon solar cells", Prog. Photovolt: Res. Appl. 13 (2005) 27.