18.1% EFFICIENCY FOR A LARGE AREA, MULTI-CRYSTALLINE SILICON SOLAR CELL.

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ABSTRACT

Multi-crystalline silicon has dominated the photovoltaic market in recent years and with advances in isotexturing and the production of increasingly thinner and larger wafers it is set to play a significant role in the future. As with other cell types, laboratory efficiencies remain higher than those achieved in production. Previous large area efficiency records on multi-crystalline silicon have included a 17.6% efficient cell produced at the University of Konstanz and a 17.7% efficient cell produced by Kyocera. The 17.6% cell was made using the buried contact technique. Again using this technique and multi-crystalline silicon, we have made an 18.1% efficient cell, independently confirmed by the calibration laboratories at Fraunhofer ISE. The area of the cell is 137.7 cm^2; V_{oc} is 636 mV and J_{sc} is 36.9 mA/cm^2. To the best of our knowledge, this is a new world record.

INTRODUCTION AND BACKGROUND

Multi-crystalline silicon is an important material for the photovoltaic industry. Crystalline silicon has a 93% share of the photovoltaic market [1] of which multi-crystalline silicon forms the majority. Multi- is cheaper than mono-crystalline silicon, but results in lower cell efficiencies primarily due to increased recombination at the crystallographic boundaries. Most commercial production on multi-crystalline silicon is done using a screen printed process, on mono-crystalline silicon, production is more varied and commercial processes include a buried contact process.

The buried contact technique is a high efficiency cell design that was first introduced by Wenham and Green at the University of New South Wales [2]. The process typically results in higher efficiencies than a screen printed process because of the selective emitter design and reduced front surface shading losses (approximately 4%, compared with 7-8% for screen printed cells). Buried contact cells are currently produced commercially on mono-crystalline silicon by BP Solar at their facilities in Tres Cantos, Spain, where over 80MW$_p$ have been produced since 1992 [3]. Commercial production is not done on multi-crystalline silicon, but in earlier work, we have demonstrated this to be feasible [4]. Figure 1 shows a schematic of a hybrid screen print / buried contact solar cell.

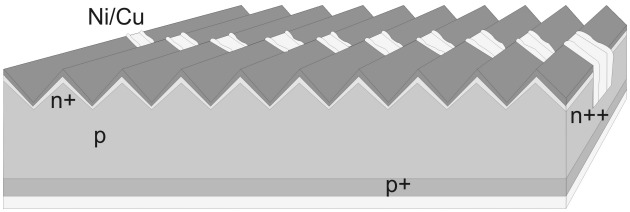


Figure 1: *Hybrid screen print / buried contact solar cell design. The cell has a selective emitter and low pressure chemical vapour deposition (LPCVD) SiN_x is used for the front surface anti-reflection coating (ARC). The back surface field (BSF) is formed by screen printing an Al layer.*

Table 1 lists high efficiency cell results for large area cells on multi- and mono- crystalline silicon and the overall record for multi-crystalline silicon.

Efficiency (%)	Area (cm^2)	Material & Doping (Ωcm)	Cell concept	Ref.
17.6	144	mc 0.5	Buried contact	[5]
17.7	232.5	mc 0.5-2.0	Screen printed	[6,7]
17.0	156	mc	Screen printed	[8,9]
20.3 (18.1)*	1 (60)	mc 0.6	Photolitho-graphy	[10,11]
18.3	147.5	(Cz)	Buried contact (Pilot-line)	[12]
21.5	100.3	n-type Cz	HIT	[13,14]
21.5	148.9	FZ	IBC	[13, 15]

Table 1: *Previous high efficiency cell results for large area cells and the overall record for multi-crystalline silicon. *Reported as a mean value for 60 cells of 1 cm^2 from two wafers.*

SOLAR CELL PROCESS

Starting with 0.5 Ωcm Polix multi-crystalline silicon from Photowatt, we used the hybrid screen print / buried contact process developed at the University of Konstanz [16] and shown in Figure 2. The first step was mechanical V-texturing of the front surface. The grooves were made using a blade with a 60º angle and were approximately 50 µm deep and spaced 100 µm apart. The next steps were a light phosphorous diffusion, resulting in a 100 Ω/sq emitter, and deposition of an 110 nm thick SiN_x layer using low pressure chemical vapour deposition (LPCVD). The SiN_x later formed the front anti-reflection coating, and the initial deposition was thicker to allow for the consumption that occurred during the heavy groove diffusion. Wafers were placed back-to-back during the nitride deposition. During this process there is often some "creep-around", which results in deposition on the edges of the rear surface. This was removed by a rear surface plasma etch.

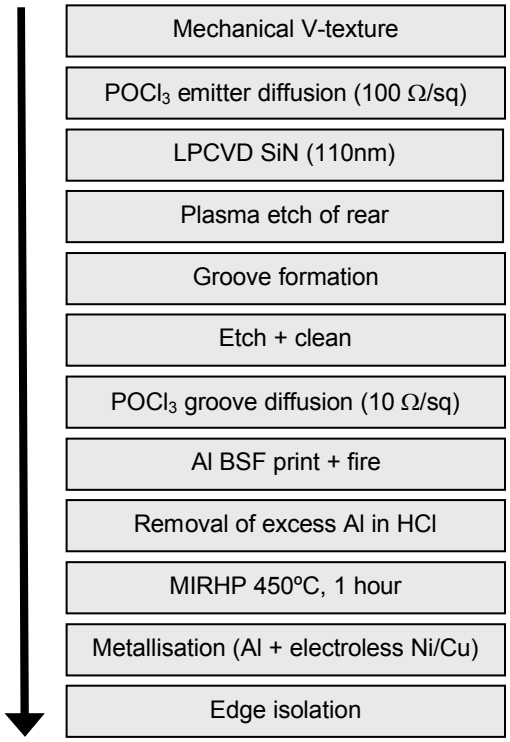


Figure 2: *Processing sequence for the high efficiency hybrid screen print / buried contact cells.*

Groove formation was done mechanically, using an ultra-thin (15 µm) blade. After a groove damage etch, the groove width was approximately 20 µm, which is much thinner than the 50 µm typically achieved in industry using a laser [17]. The next step was a heavy phosphorous diffusion, which resulted in a 10 Ω/sq emitter in the grooves and on the rear and also gettered the material. During this step and the subsequent deglaze, the LPCVD SiN_x thickness was reduced to approximately 75 nm. Following this, a full area aluminium back surface field (BSF) was screen printed onto the rear of the wafer. After firing (which results in an out-gettering of the phosphorous on the rear [18]), the excess aluminium was removed in an HCl acid etch. This step requires handling of individual wafers and in an industrial environment it would result in the production of large amounts of an Al-paste/HCl slurry that would need to be filtered for reuse or disposed. In previous work, we have shown that it is possible to process high efficiency buried contact cells on multi-crystalline silicon avoiding this step [4].

The next step was a 450ºC, 1 hour treatment in our Microwave Induced Remote Hydrogen Passivation (MIRHP) system to introduce hydrogen (for passivation) into the wafer bulk. Following this, a 2 µm thick Al layer was evaporated on the rear as an aid to our plating. Metallisation was done using electroless deposition of Ni and then Cu. Metal was deposited in the front grooves and on the full rear surface. A metallization sequence suitable for commercial production is electroless deposition of Ni, followed by a Ni sinter and then electroless deposition of a second Ni layer, Cu and Ag. Lastly, edge isolation was done using a dicing saw.

SOLAR CELL RESULTS

IV measurements of the best cell were made at the Fraunhofer ISE CalLab. The cell area was confirmed to be 137.7 cm^2, V_{oc} to be 636.0 mV, J_{sc} to be 36.91 mA/cm^2 and fill factor to be 77.0%, resulting in an efficiency of 18.1%. These cell results are compared to our previous best cell [5], also measured at the Fraunhofer ISE CalLab in Table 2. The cells were made from near-neighbouring wafers from the same block of the same ingot, as can be seen in Figure 6.

Area (cm^2)	d (µm)	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF (%)	η (%)
144.0	240	35.9	632.5	77.7	17.6
137.7	310	36.9	636.0	77.0	18.1

Table 2: *IV data for the best cell from our current batch compared with our previous best cell.*

Compared to our previous best cell, this new cell shows a large improvement in J_{sc} (1.0 mA/cm^2), a small increase in V_{oc} (3.5 mV) and a decrease in fill factor. The net result is an absolute efficiency gain of 0.5%.

ANALYSIS

In order to understand the reason behind the 0.5% absolute gain in cell efficiency, we have made a more detailed comparison of the two cells.

Firstly, we examined the profile of the front surface texture. Figure 3 shows microscope images taken side-on for both cells. In the case of the 18.1% efficient cell, the texture is deeper (~55 µm compared to ~40 µm for the 17.6% efficient cell) and "pointier" at the base of the grooves. Another physical difference between the two

cells is the thickness; 310 µm in the case of the 18.1% cell and 240 µm in the case of the 17.6% cell.

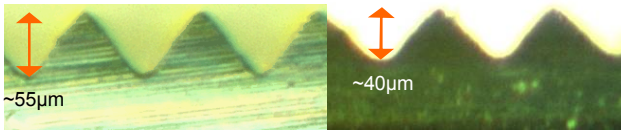


Figure 3: *Microscope images showing the difference in front surface texture for the two cells. On the left is the 18.1% efficient cell, on the right the 17.6% efficient cell.*

The difference in front surface texture should be evident in a measurement of reflectance as a function of wavelength and this is shown in Figure 4 for both cells. The better (deeper and pointier) texture of the 18.1% efficient cell is evident in the flatter curve in the wavelength region 600-1000 nm. The 18.1% efficient cell has a higher rear reflectance as evidenced by the higher reflection at long wavelengths. At short wavelengths, however, the 17.6% efficient cell has a lower reflectance, possibly due to a more optimal nitride thickness.

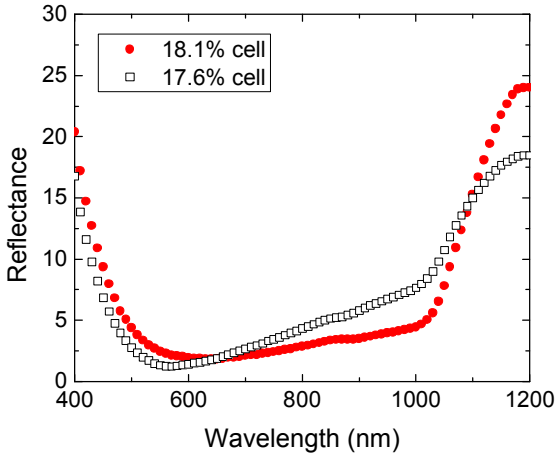


Figure 4: *Reflectance as a function of wavelength for the two cells. The closed symbols represent the 18.1% efficient cell, the open symbols the 17.6% efficient cell.*

The internal quantum efficiency (IQE) of the two cells was also measured and the results are shown in Figure 5. These results show a higher IQE for the 18.1% efficient cell at longer wavelengths, suggesting a better bulk diffusion length. The same result is evident in laser beam induced current (LBIC) measurements of the two cells. Figure 6 shows LBIC measurements at 980 nm converted to an EQE for both cells. In both cases the multi-crystalline structure is evident and again, the 18.1% efficient cell appears to have a better bulk diffusion length.

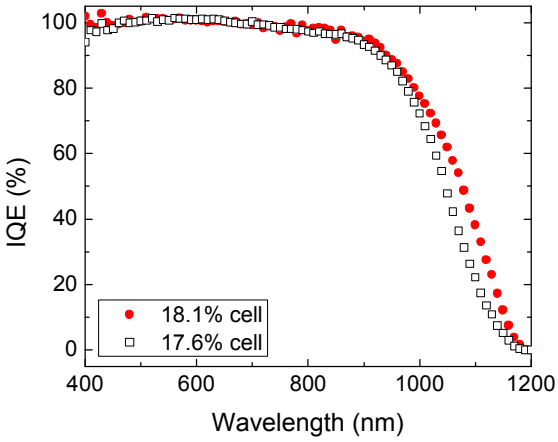


Figure 5: *IQE as a function of wavelength for the two cells. The closed symbols represent the 18.1% efficient cell, the open symbols the 17.6% efficient cell.*

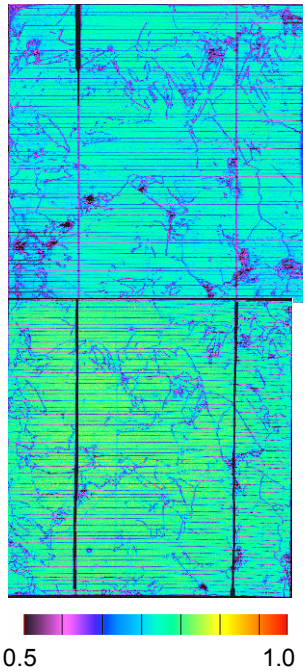


Figure 6: *LBIC measurements. Shown is the EQE at 980 nm for the 17.6% efficient cell (above) and the 18.1% efficient cell (below).*

Using a program similar to IQE1D [19] (called "SR" and written by Fischer [20]) the IQE was fitted to extract the rear surface recombination velocity, S_{rear}, and the bulk diffusion length, L_{diff}, and the reflectance was fitted to extract the rear surface reflectance, R_{rear}. These values are shown in Table 3 for the two cells.

Parameter	17.6% cell	18.1% cell
S_{rear} (cm/s)	1010	765
L_{diff} (µm)	250	330
R_{rear} (%)	60	75

Table 3: *Values for S_{rear}, R_{rear} and L_{diff} fitted to the IQE curves of the 17.6% and 18.1% efficient cells.*

The excess charge carrier concentration profile in the emitter can be determined using an electrochemical capacitance voltage (ECV) measurement. Since this is a destructive technique, an ECV measurement was made on a similarly diffused wafer and assumed to be the same for both the 17.6 and 18.1% efficient cells, a reasonable assumption since the wafers had the same emitter diffusion. ECV measured profiles for both the groove (measured using the surface of a dummy wafer) and emitter are shown in Figure 7.

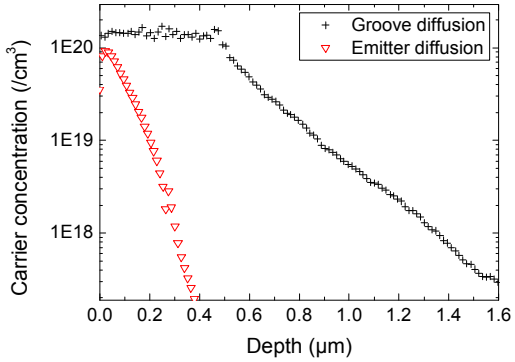


Figure 7: *ECV measurement of the buried contact emitter and groove diffusions.*

The measured or fitted parameters of the two cells were then used in the simulation program PC1D [21] to obtain two PC1D models; PC1D_17.6 and PC1D_18.1. PC1D_17.6 was modified, one parameter at a time, to determine the influence of the different parameters on the J_{sc} and V_{oc} values. In order to account for the regions with a heavy groove diffusion, the cell was assumed to consist of the region with a light phosphorous diffusion connected in parallel to a diode shunt with an I_0 of 10^{-13} A. The V_{oc} values predicted by the PC1D models are very close to the measured values and the J_{sc} values are approximately 2% higher than the measured J_{sc}. Since this is consistent for both cells, we looked at the change in V_{oc} and J_{sc}. The results are shown in Table 4 together with the change in efficiency, assuming a fill factor of 77.7% (the measured fill factor of the 17.6% efficient cell).

Parameter	Change	Δ V_{oc} (mV)	Δ J_{sc} (mA/cm^2)	Δ eff (%)
Thickness (µm)	240→310	0	0	0
Text deptj (µm) & Ref	40→55 18.1% Ref	-0.1	+0.1	+0.1
L_{diff}	250→330	+2.8	+0.3	+0.3
S_{rear}	1150→770	+0.6	+0.1	+0.1
R_{rear}	60→75	+0.2	+0.3	+0.2
Total (modeled)		+3.9	+0.9	+0.5
Total (measured)		+3.5	+1.0	+0.5

Table 4: E*ffect of the differences between the 17.6% efficient cell and the 18.1% efficient cell on J_{sc}, V_{oc} and efficiency (assuming a fill factor of 77.7%).*

The PC1D modeling suggests that the difference between the two cells is primarily due to an increased bulk diffusion length and a better rear surface for the 18.1% efficient cell.

FUTURE POSSIBILITIES

PC1D_18.1 was used to estimate the future efficiency that may be achieved in a research environment and in an industrial environment.

High Efficiency Future

There is substantial room for improvement in the fill factor and the 18.1% efficient cell suffered due to a non-optimal plating procedure. Using a similar plating process, we have previously achieved fill factors of up to 78.8% [4] and a fill factor of 79.0% does not seem unrealistic. With this improvement alone, the cell efficiency would be boosted to 18.5%.

The reflectance for the 17.6% efficient cell is slightly better in the short wavelength region, probably as a result of a slight difference in silicon nitride thickness for the two layers. An improvement in cell efficiency could be expected with a more optimized reflectance, which in practice could be achieved using the cell texture of the 18.1% efficient cell and the nitride thickness of the 17.6% efficient cell. As a first approximation of this, a reflectance equal to that of the 17.6% efficient cell at lower wavelengths and the 18.1% efficient cell at higher wavelengths was used in the PC1D models. This resulted in an increase in V_{oc} of 0.2 mV and in J_{sc} of 0.2 mA/cm^2.

The cell efficiency could be improved by an improved rear surface. This is currently an important topic for screen printed cells [22], which have a similar rear structure, especially with the trend to thinner wafers. An improved rear surface may be achieved using a local contacting scheme, which would allow both a decreasd S_{rear} and an increased R_{rear}. Assuming values for S_{rear} of 200 cm/s and R_{rear} of 95%, which is moderately conservative for a local contact scheme (see, for example, [22]) results in an improvement in V_{oc} of 1.2 mV and in J_{sc} of 0.2 mA/cm^2 if only S_{rear} is improved and improvements in V_{oc} and J_{sc} of 0.2 mV and 0.4 mA/cm^2 respectively if only R_{rear} is improved. With both improvements, an increase of 1.5 mV in V_{oc} and of 0.6 mA/cm^2 in J_{sc} could be expected.

The lifetime of the material is already very high (average approximately 47 µs) and the diffusion length is comparable to the wafer thickness. Nevertheless, the material was part of a standard batch and if only a small increase in L_{diff} is possible, for example to 360 µm (equivalent to an average bulk lifetime of ~56 µs), a 0.6 mV increase in V_{oc} and a 0.1 mA/cm^2 increase in J_{sc} may be expected.

There is also room for improvement in front surface passivation since at present this is only provided by a LPCVD SiN_x layer deposited directly onto silicon (the phosphorous glass is removed after the initial, light

diffusion). Our analysis suggests S_{front} is approximately 14 000 cm/s (equivalent to a J_0 of ~80 fA/cm^2), reducing this to 8 000 cm/s (J_0~45 fA/cm^2), for example with the careful use of an oxide/nitride stack [23] so as not to unnecessarily increase the thermal budget and therefore degrade the bulk lifetime, could result in an increase in V_{oc} of 2.7 mV and in J_{sc} of 0.1 mA/cm^2, provided the oxide layer is kept thin to minimize any increase in reflectance [24].

Another high efficiency improvement that may be implemented is the use of the zero-shading loss cell design; ABC (angled buried contact) [25]. This cell design relies on angled front contacts and a directionally deposited dielectric and is shown in Figure 8. Since the 18.1% efficient cell has metallization covering approximately 3% of the front surface, application of the ABC cell design would result in an increase in J_{sc} of 1.1 mA/cm^2, leading to a total efficiency of 19.1%.

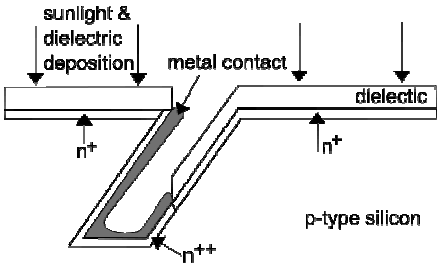


Figure 8: Side view of t*he ABC (Angled Buried Contact) cell design. Front contacts are angled into the wafer and, when combined with a directionally deposited dielectric, the result is negligible front surface shading losses.*

Table 5 shows a summary of the improvements in J_{sc}, V_{oc} and efficiency that may be achieved by implementation of each of the improvements mentioned above. When all of the high efficiency improvements are combined, a large area cell efficiency of 20% may be achieved.

Change	New value	Δ V_{oc} (mV)	Δ J_{sc} (mA/cm^2)	Effic. (%)
Fill factor	79%			18.5
Improved reflectance		+0.2	+0.2	18.6
Local contacts	S_{rear} = 200cm/s R_{rear} = 95%	+2.5	+1.0	19.1
Bulk	L_{diff} = 360 µm	+0.9	+0.1	18.6
Front passivation	S_{front} = 8000 cm/s	+2.6	+0.1	18.7
ABC cell design	Shading loss = 0%	0	+1.1	19.1
Total		+6.9 (642.9)	+2.7 (39.6)	20.1

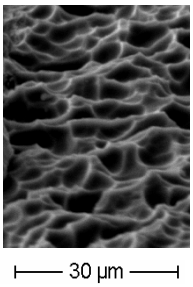
Table 5: *A summary of the effect of each of the improvements listed above on J_{sc}, V_{oc} and efficiency, assuming a fill factor of 79%. The sum of the improvements is not equal to the total improvement, since the response is non-linear.*

Industry Future

The cell efficiency that could be achieved using an industrially compatible process was modeled with the following assumptions:

- Cell thickness 200 µm;
- Front surface shading ~4%;
- An isotextured front surface. An isotexturing process suitable for application to multi-cystalline silicon was developed at the University of Konstanz [26] and together with the company Rena, this process has been further developed for use in industry [27]. Figure 9 shows a scanning electron microscope image of an isotextured surface. Figure 10 shows a comparison of reflectance as a function of wavelength for an isotextured buried contact cell and the 18.1% efficient cell.

Figure 9: *Scanning electron microscope image of an isotextured front surface.*



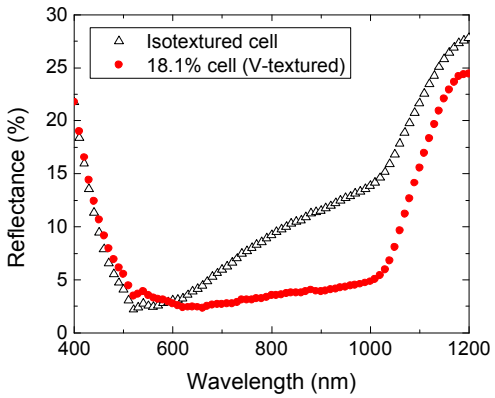


Figure 10: *Reflectance measurements for an isotextured buried contact cell compared with the 18.1% efficient cell.*

Other aspects that must be considered for an industrial process are the HCl etch step and bulk hydrogen passivation. The HCl step is used in our process to remove excess aluminium after the screen print and fire. The application of this step will affect when hydrogenation can be done and the quality of the material will determine the benefits of hydrogenation.

Two PC1D models were made, the first with an L_{diff} of 330 µm (as measured for the 18.1% efficient cell) and the second with an L_{diff} of 200 µm. The results are shown in Table 6.

L_{diff}	V_{oc} (mV)	J_{sc} (mA/cm^2)	Efficiency (%)
330 µm	635	35.1	17.6
200 µm	630	34.6	17.2

Table 6: *V_{oc}, J_{sc} and efficiency (assuming a fill factor of 79%) values that may be achieved with an industrial process.*

The results shown in Table 6 are indicative of the cell efficiency that may be achieved using existing technology. Industrial efficiencies may reach the 18% presented in this paper, if, for example, J_{sc} is improved to approximately 36 mA/cm^2 using an innovative approach, such as a multiple layer SiN_x stack for the front surface anti-reflection coating or by using a part-ABC process (only the fingers angled into the wafer) or by application of a locally contacted rear surface. Cell efficiencies may also reach the 18% mark if the high bulk diffusion length can be maintained with a low (approximately 0.2 Ωcm) resistivity substrate.

CONCLUSIONS

We have presented a cell result, which, as far as we know, is a new world record for large area, multi-crystalline silicon. The cell has an independently confirmed efficiency of 18.1%. It has an area of 137.7 cm^2, a V_{oc} of 636.0 mV and a J_{sc} of 36.91 mA/cm^2. The improvement over our previous best cell efficiency is largely due to an increased bulk diffusion length and to a better rear surface. Simple modeling predicts that a large area, multi-crystalline silicon cell efficiency of over 20% should be achievable in the laboratory and 17.6% in industry using existing techniques or 18.0% with some innovation.

ACKNOWLEDGEMENTS

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