Compensation of the Sputter Damage During a-Si Deposition for poly-Si/SiO$_x$ Passivating Contacts by Ex-Situ P-Doping

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**Abstract.** The rf magnetron sputter deposition of a-Si during fabrication of passivating contacts based on poly-Si on top of an interfacial silicon oxide (poly-Si/SiO$_x$) and a possible sputter damage similar to the one observed during transparent conductive oxide (TCO) sputtering for heterojunction solar cells is investigated. It is shown that the high temperature anneal for partial crystallization of the sputtered a-Si has a detrimental effect on passivation quality in contrast to the known beneficial annealing after TCO sputtering for heterojunction solar cells. However, doping during crystallization of the a-Si layer by a POC$_1$$_2$-diffusion compensates this decrease of passivation quality by a field effect and a beneficial diffusion of dopants through the interfacial oxide into the c-Si substrate. Moreover, a subsequent hydrogenation of the interface leads to implied open circuit voltages of up to 719 mV and saturation current densities of down to 9 fA/cm$^2$. From this it is concluded, that a beneficial annealing is only possible with the presence of hydrogen at the interface. Furthermore, depth profiles of the dopants measured by glow discharge optical emission spectroscopy (GD-OES) and electrochemical capacitance-voltage profiling (ECV) reveal a significant gap in atomic density $n_p$ between total ($3.5\times10^{21}$ cm$^{-3}$) and electrically active ($5\times10^{20}$ cm$^{-3}$) phosphorous atoms in the poly-Si layer. Both values are higher than the corresponding limits of phosphorous in poly-Si, which could be explained by mobile inactive phosphorous and the formation of monoclinic SiP precipitates. From these depth profiles also a pile-up of electrically inactive phosphorous close to, but a few nanometers off the interfacial oxide was observed.

**INTRODUCTION**

Recently, passivating contacts based on doped poly-Si layers on top of an interfacial oxide (poly-Si/SiO$_x$) are successfully applied in high efficiency solar cells [1]. There are several amorphous silicon (a-Si) deposition techniques available, e.g. chemical vapour deposition [1], electron beam evaporation [2] or sputter deposition [3]. Up to now it is not clear which technique will be able to produce high efficiency solar cells and at the same time offer a sufficient industrial throughput. In this contribution, the a-Si deposition by rf magnetron sputtering is investigated as this technique is already established for high industrial throughput.

One challenging issue is a possible sputter damage to the passivated interface, as it is known from sputtering of transparent conductive oxides (TCO) for heterojunction solar cells. There are two main sources of this damage, first plasma irradiation by high energy photons and second particle bombardment by sputtered atoms, reflected neutrals, ions and electrons [4]. The strength of these damage sources can be controlled by the sputter parameters, i.e. low plasma power, high plasma pressure, large target-sample distance and high substrate temperature [4,5].

In case of TCO sputtering it was reported that a thermal treatment at moderate temperatures may compensate the induced sputter damage [4,5]. For poly-Si/SiO$_x$ passivating contacts a thermal treatment at high temperatures is inherently included in the fabrication process to partly crystallize the a-Si. Up to now it is not clear if this high...
temperature anneal is able to compensate the sputter damage to the passivated interface similar to the comparatively colder thermal treatment after TCO sputtering.

**EXPERIMENTAL**

The used substrate was 250 µm thick n-type silicon floating zone with a base resistivity of 200 Ωcm cut into 5x5 cm² pieces. Immediately after a short dip in hydrofluoric acid (HF), an interfacial oxide was thermally grown with a thickness of roughly 2.5 nm. a-Si layers with a thickness of approximately 75 nm were rf magnetron sputtered successively on both sides of the samples with a pure argon plasma applied to an undoped silicon target with a purity of 99.999%. The sputter parameter set was optimized with respect to a trade-off between low sputter damage and a sufficient deposition rate.

One group of these intrinsic a-Si layers was partially crystallized in a quartz tube furnace in N₂ atmosphere while the other group was doped via POCl₃ diffusion. Both high temperature anneals were operated above 900°C for 30 min immediately after an H₂O₂/HCl and HF cleaning process. Afterwards, the grown phosphorous silicate glass was removed with HF and subsequent spectral ellipsometry measurements revealed a reduced poly-Si layer thickness of roughly 67 nm. For hydrogenation, on one half of the samples a silicon nitride was plasma-enhanced chemical vapour deposited on both sides and a subsequent firing step was performed in a belt furnace at a peak set temperature of 910°C.

All samples were characterized by photoconductance decay (PCD) measurements in terms of implied open circuit voltages iV_{oc}, saturation current densities J₀ and sheet resistance Rₛ. In addition, depth profiles of the total phosphorous atomic density and uncalibrated oxygen content were determined using glow discharge optical emission spectroscopy (GD-OES). The oxygen measurements suffer from atmospheric contamination signals in the first measurement seconds, which were corrected following the method described in [6]. Depth profiles of the electrically active phosphorous atomic density were determined using electrochemical capacitance-voltage profiling (ECV). In such measurements, the thickness of the poly-Si layer is usually underestimated, which can be attributed for with a valency correction. For c-Si material a typical value of 3.7 is used, which was adjusted in this study to a value of 1.48 so that the profile depth matches the poly-Si layer thickness determined by spectral ellipsometry.

**RESULTS AND DISCUSSION**

*Sputter Damage Compensation*

After each process step, samples were taken and characterized in terms of iV_{oc}, as summarized in Fig. 1. One sample with an as-grown interfacial oxide acts as reference with iV_{oc} = 621 mV.

![FIGURE 1. iV_{oc} after each process step. The square corresponds to the reference sample with the as-grown interfacial oxide, triangles to intrinsic layers and circles to doped layers.](image-url)
The a-Si sputter deposition reduces $iV_{oc}$ by 10 mV. This behaviour is interpreted as a result of the sputter damage to the interface between the interfacial oxide and the c-Si substrate by plasma irradiation and particle bombardment.

The following high temperature anneal to partially crystallize the a-Si layer further decreases $iV_{oc}$ to values below 600 mV. Hence, it seems that a beneficial annealing process similar to the one after TCO sputtering is not possible for poly-Si/SiO$_2$ passivating contacts within the standard process flow, most probably due to the lack of hydrogen in sputtered a-Si layers. It was previously reported that, in addition to the partial crystallization of the a-Si during the high temperature anneal, local breakups of the interfacial oxide form pinholes, which cause beneficial diffusion of dopants into the c-Si substrate [7]. Since the pure thermal treatment of the intrinsic sputtered a-Si layer does not provide any dopants, these pinholes might form local intrinsic poly-Si/c-Si interfaces, which could be another explanation for the loss in passivation.

From this finding it seems likely to dope the a-Si layers. To avoid an additional process step, the doping was realized by a POCl$_3$ diffusion of the a-Si, retaining the temperature and process duration of the initial high temperature anneal. The POCl$_3$ diffused samples show $iV_{oc}$ values of up to 677 mV, which are higher than the initial passivation of the as-grown interfacial oxide reference. This is explained by a field effect passivation and the above mentioned beneficial diffusion of dopants through pinholes in the interfacial oxide into the c-Si substrate [7], where they enhance passivation by reducing the recombination at these pinholes.

As sputtered a-Si is basically hydrogen-free and the thermal treatment alone did not compensate the loss in passivation quality from the sputter damage, it is reasonable to hydrogenate the sample to saturate defects at the interface to the c-Si substrate. Indeed, after deposition of hydrogen-rich silicon nitride on top of the doped poly-Si layer and a subsequent firing step, $iV_{oc}$ is increased up to an average value of 715 mV (see Table 1). For these samples it was also possible to determine saturation current densities down to $J_0 = 9 \, \text{fA/cm}^2$, which is in the range of typical values for poly-Si/SiO$_2$ passivating contacts [8].

Likewise, hydrogenation of the intrinsic samples increases $iV_{oc}$ from below 600 mV after the thermal treatment to values, which are comparable to or higher than the ones of the as-grown interfacial oxide reference. This means that the presence of hydrogen during the firing step is able to compensate the loss in passivation quality from the sputter damage, probably by passivation of the local intrinsic poly-Si/c-Si interfaces mentioned above. Similarly, during the beneficial annealing after TCO sputtering for heterojunction solar cells, hydrogen from the chemical vapour deposited a-Si:H layers is permanently located at the passivating interface. Hence, it seems reasonable that the presence of hydrogen is a general condition for compensation of a sputter damage.

### TABLE 1. Summary of the average and best values of the POCl$_3$-diffused samples after SiN$_x$ hydrogenation.

<table>
<thead>
<tr>
<th></th>
<th>$iV_{oc}$ [mV]</th>
<th>$J_0$ [fA/cm$^2$]</th>
<th>$R_s$ [\Omega/\square]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average</td>
<td>715</td>
<td>9.3</td>
<td>257</td>
</tr>
<tr>
<td>Best value</td>
<td>719</td>
<td>8.7</td>
<td>243</td>
</tr>
</tbody>
</table>

**Dopant Depth Profiles**

All POCl$_3$ diffused poly-Si layers show similar elemental depth profiles independent whether hydrogenated or not. Figure 2 shows these profiles for one sample exemplarily.

The most obvious observation is the large gap in atomic density $n_p$ between total ($\sim 3 \times 10^{21}$ cm$^{-3}$, measured by GD-OES) and electrically active ($\sim 5 \times 10^{20}$ cm$^{-3}$, measured by ECV) phosphorous atoms in the poly-Si layer. The ECV measured atomic density is higher than the limit of electrically active phosphorous in poly-Si equilibrated at 900°C of roughly 3.35-$10^{20}$ cm$^{-3}$ (see grey dashed horizontal line in Fig. 2) according to [9]. Similar values above this limit were reported before [10]. A possible explanation for this behaviour is that the ECV etch process etches faster at grain boundaries and consequently the effectively etched area is increased. A correction for this larger etched area would lower the measured atomic densities. Due to lack of clear evidence, in this study such a correction was not applied.

The hypothesis that the ECV measured atomic density has to be adjusted in height is supported by cross-checking the electrically active atomic density of phosphorous starting from the average sheet resistance of $R_s=257 \, \Omega/\square$ (see Table 1) under the assumption of a constant atomic density throughout the whole layer via the following equation:

$$n_p = (R_s \cdot \mu_e \cdot d \cdot e_0)^{-1}$$  \hspace{1cm} (1)
FIGURE 2. Depth profiles of a POCl₃-diffused sample after SiNₓ hydrogenation. Total phosphorous atomic density (solid black line) and uncalibrated oxygen content (solid light blue line) measured by GD-OES. Vertical lines are the positions of the respective peak maximums. The peak in the oxygen signal represents the position of the interfacial oxide between the poly-Si layer (left) and the c-Si substrate (right). Depth profile of electrically active phosphorous atomic density measured by ECV (red error bars, dotted line as guide for the eye). The grey dashed horizontal line is the limiting atomic density of electrically active phosphorous in poly-Si equilibrated at 900°C according to [9].

With \( \mu_e = 11.4 \, \text{cm}^2/\text{As} \) the electron mobility from Hall effect measurements, \( d = 67 \, \text{nm} \) the layer thickness and \( e_0 \) the elementary charge, the atomic density is determined to \( n_0 = 3.18 \times 10^{20} \, \text{cm}^{-3} \), which is closely below the limiting value from [9].

The atomic density measured by GD-OES is also higher than the limit of total phosphorous atomic density in poly-Si of roughly \( 5.34 \times 10^{20} \, \text{cm}^{-3} \) according to [9], but similarly high values were also reported before from secondary ion mass spectroscopy (SIMS) [11] and from secondary neutral mass spectroscopy (SNMS) [9]. The authors in [9] used ion implantation reaching total atomic densities of up to \( 10^{22} \, \text{cm}^{-3} \) and explained these high values with mobile inactive phosphorous and the formation of monoclinic SiP precipitates. This explanation could also apply for the GD-OES profile presented in Fig. 2. Furthermore, the presence of SiP precipitates might also contribute to the high atomic density measured by ECV above the limit if the assumption of a well-defined silicon lattice does not apply.

In the oxygen signal a clear peak was measured, which originates from the interfacial oxide. Likewise, a pile-up of phosphorous in the GD-OES profile is observed. From the vertical lines in Fig. 2 it is evident that the phosphorous peak appears shortly before the oxygen peak, meaning that the pile-up is close to, but a few nanometers off the interfacial oxide. A similar pile-up is not present in the ECV depth profile of the electrically active phosphorous, leading to the conclusion that the pile-up consists of electrically inactive phosphorous only. Such a pile-up of electrically inactive phosphorous at a Si/SiO₂ interface was reported before [12]. This finding is also compatible with the above mentioned formation of monoclinic SiP precipitates as reason for the pile-up.

The above mentioned diffusion of dopants into the c-Si substrate is not clearly visible in the depth profiles in Fig. 2. The profile measured by GD-OES reaches the detection limit in the range of \( \sim 10^{19} \, \text{cm}^{-3} \). The detection limit of ECV measurements is in principle below \( 10^{16} \, \text{cm}^{-3} \) and hence a deeper diffusion profile compared to the one in Fig. 2 would be expected. However, complications during the ECV etch process in the c-Si region near the interfacial oxide led to ambiguous data points, which is why the profile in Fig. 2 only shows data points down to \( \sim 10^{19} \, \text{cm}^{-3} \).

CONCLUSION

The a-Si deposition from rf magnetron sputtering causes a sputter damage to the interface of the poly-Si/SiOₓ passivating contact. A thermal treatment compensates this damage only if phosphorous is offered during partial
crystallization by a POCl₃-diffusion, leading to a field effect passivation and a beneficial diffusion of dopants through pinholes in the interfacial oxide into the c-Si substrate, or if hydrogen is offered during hydrogenation. Depth profiles of the doped poly-Si layers reveal a significant gap in atomic densities nP between the total and electrically active phosphorous in the poly-Si layer. Both measured values were higher than the respective limits for atomic densities of phosphorous in poly-Si, which could be explained by mobile inactive phosphorous and the formation of monoclinic SiP precipitates. Additionally, a pile-up of electrically inactive phosphorous is observed close to, but a few nanometers off the interfacial oxide.

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